# Electrostatic control of insulating $SrTiO_3$ surface: insulator-metal transition, negative capacitance, multi-band conduction, Kondo effect, and more.

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Most of the people in the world have not given it a thought that our fully electronics-depended society is now really confronted a fatal problem called "miniaturisation limit" of transistors. By the time of Tokyo Olympic in 2020, it is anticipated a typical dimension of the transistor would reach 10 nm. Then, the channel contains only about 10 chemical dopants (origin of carriers), and the switching energy becomes smaller than the thermal noise limit ($\sim 100\, k_B T$); "on/off" states are no more distinguished. The saviour from such a looming crisis is nothing but to use a chemical-doping-free FET, and to develop such electronics beyond the present Si ones is indeed an urgent challenge for condensed matter physicists.

In this talk, we demonstrate an example: by applying an electric field, a quite insulating 'non-doped' $SrTiO_3$ shows a two dimensional (2D) insulator-metal transition at the surface, and it actually works as an excellent field effect transistor (FET) with sufficiently good sub-threshold swing ($\sim$ 170 mV/decade) and very large carrier mobility ($\sim 10\,cm^2/Vs$). $SrTiO_3$ is well-known for its defect-prone surface, but by inserting a thin (6 nm) organic insulator Parylene-C between the surface and the high-$k$ gate insulator $HfO_2$, we can avoid any damages on the surface during the device fabrication as well as during the application of the gate voltage.

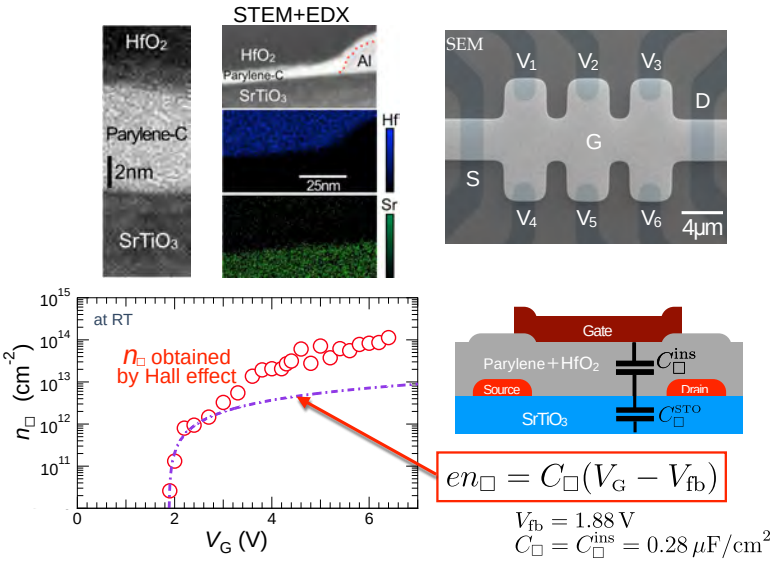


Figure 1: Cross-section TEM, and STEM & EDX indicating little mixture of the ions at the interfaces (top left). SEM of an FET device used for the Hall measurement (top right). Sheet carrier density $n_\square$ vs. $V_G$ (bottom).

This clean interface between Parylene-C and $SrTiO_3$ is not only promising for the electronic application of the $SrTiO_3$-FET but also unexpected intriguing electronic properties of the $SrTiO_3$ surface are getting revealed one after another. We can accumulate 2D carriers more than $10^{14}\,cm^2$, which is surprisingly beyond the value expected from the capacitance of the gate insulator (the phenomenon is called "negative capacitance" see Fig. 1) [1]. By increasing the gate voltage $V_G$, the channel resistance decreases, and the temperature dependence exhibits a clear insulator to metal transition with the boundary at the quantum resistance. Metallic channel shows the Kondo effect at low temperatures, as well as an anomaly of the Hall effect without hysteresis is accompanied. All these results suggest consistently the lifting of the three-fold degenerate $t_{2g}$ band, which is most probably caused by a strong Rashba effect at the surface. We will explain these phenomena with the experimental data, and discuss on the rich physics behind them.

## Brief Biography

Isao H. Inoue received BSc, MSc, and DSc degrees in Physics from the University of Tokyo in 1990, 1992 and 1998, respectively. He became a tenure researcher of the Electrotechnical Laboratory (ETL) in 1992 and a senior researcher in 1999. From 1999 to 2001, he was a visiting scholar at Cavendish Laboratory, University of Cambridge. In 2001, ETL was re-organized to the National Institute of Advanced Industrial Science and Technology (AIST); since then, he has been a senior researcher of AIST. He studied in a wide range of research field: from the high-energy spectroscopies and fermiology of strongly correlated materials to the development of the Mott transistor, ReRAM, and other electronic devices, which utilise functional oxides, where electron correlations play a crucial role.

## References

[1] N. Kumar, A. Kitoh and I. H. Inoue, *Scientific Reports* **6**, 25789 (2016).